REMARKS

Examiner James Mitchell is thanked for carefully examining and reviewing the subject patent application. The claims and the specifications have been amended in accordance with the Examiner's kind suggestions, and all claims are now believed to be in condition for allowance.

Reconsideration of Claims 34 - 39 as being rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the Applicant regards as his invention, is requested, in light of the following.
(ref. Office action 11/08/01, paragraphs 2-5)

Claims 34, 35, 37 and 38 have been amended to better define and distinctly claim the subject matter which the Applicant regards as his invention. The language of Claims 34, 35, 37 and 38 have been changed, especially the term "plurality of bond pads" has been eliminated. In addition, the specifications have been amended to reflect changes made to the claims and an addition figure has been added, Figure 5. Figure 5 is a top view depicting a sketch of a cutout section of a chip or die layout, showing multiple bond pads with individual interlocking grid arrays, for each conducting bond pad formed. (FIG. 5 enclosed)

Reconsideration of Claims 34, rejected under 35 U.S.C. 102(b), as being unpatentable over Yoshioka (U.S. 5,357,136) hereafter referred to as Yoshioka, is requested, in light of the following.

(ref. Office action 11/08/01, paragraphs 6-8)

In reviewing Yoshioka, the Applicant's interlocking grid array, of passivating material and conducting material for the bond pad structures seems not to be disclosed, neither in the Yoshoka specifications, nor in the claims. The Applicant's invention, in the specifications and in Claims 34 and 37, the invention provides details of the conducting bond pad formed by the interlocking grid array, giving detailed dimensions, e.g., approximately 100 by 100 microns square and the size of the structures are from about 10 to 25 microns in width, approximately 4 microns in height, and from about 4 to 10 in number, per conducting bond pad, thus, increasing surface area for improved adhesion.

Reconsideration of Claims 34 and 36, rejected under 35 U.S.C. 102(b), as being unpatentable over Camilletti (U.S. 5,693,565) hereafter referred to as Camilletti, is requested, in light of the following.

(ref. Office action 11/08/01, paragraphs 6,9,10)

In reviewing Camilletti, there are no comparable bond pad structures disclosed that are similar to that of the Applicant's invention. Some elements of semiconductor technology overlap in invention claims, and are common elements. However, in the Applicant's Claims 34 and 36, the passivating layer is selected from the group consisting of SiO, SiN, and polyimide. Furthermore, in the Applicant's invention, the key application is forming an interlocking grid array for bond pad formation. In contrast, Camilletti's invention focuses on using hydrogen silsequioxane resins to better connect and anchor conventional bond pads.

Reconsideration of Claims 36 and 34, rejected under 35 U.S.C. 103(a), as being unpatentable over Yoshioka, in view of Camilletti, is requested, in light of the following.
(ref. Office action 11/08/01, paragraphs 11-14)

Please find similar counter arguments, as above, namely:

In reviewing Camilletti, there are no comparable bond pad structures disclosed that are similar to that of the Applicant's invention. Some elements of semiconductor technology overlap in invention claims, and are common elements. However, in the Applicant's Claims 34 and 36, the passivating layer is selected from the group consisting of SiO, SiN, and polyimide. Furthermore, in the Applicant's invention, the key application is forming an interlocking grid array for bond pad formation. In contrast, Camilletti's invention focuses on using hydrogen silsequioxane resins to better connect and anchor conventional bond pads. The Applicant's invention has key differences.

Agree that Yoshioka's invention does not show the passivating layer consisting of silicon oxide. Furthermore, the Applicant's interlocking grid array, of passivating material and conducting material for the bond pad structures seems not to be disclosed, neither in the Yoshoka specifications, nor in the claims. The Applicant's invention has key differences.

Reconsideration of Claims 39 and 34, rejected under 35 U.S.C. 103(a), as being unpatentable over Camilletti, in view of Saran (U.S. 6,232,662) hereafter referred to as Saran, is requested, in light of the following.

(ref. Office action 11/08/01, paragraphs 11, 15-17)

In reviewing both Camilletti and Saran, there are no comparable bond pad structures disclosed that are similar to that of the Applicant's invention. Some elements of semiconductor technology overlap in invention claims, and are common elements. However, in the Applicant's Claims 39 and 34, the bond pad barrier layer is formed of TiN. Diffusion barrier layers are common practice in the Industry. Furthermore, in the Applicant's invention, the key application is forming an interlocking grid array for bond pad formation, of which, for completeness and showing diligence, a barrier layer is necessary.

In conclusion, for state-of-the-art advanced applications in silicon gate technology, the applicant's invention is believed to be patentable over Prior Art references, because there seems to be insufficient basis for concluding that the modification of Prior Art disclosures, would have been obvious to one skilled in the art. That is to say, there must be something in the prior art or line of reasoning to suggest that

the combination of these various references is desirable. We believe that there is no such basis for the combination

All rejected claims are now believed to be in allowable condition, and allowance is so requested.

Attached hereto is a marked-up version of the changes made to the specifications and the claims by the current Amendment. The attached page is captioned, "Version With Markings To Show Changes Made."

It is requested that should there be any problems with this Amendment, please call the undersigned Attorney at (914) 452-5863.

Respectfully submitted,

Stephen B. Ackerman, Reg.No. 37,761

VERSION WITH MARKINGS TO SHOW CHANGES MADE

PLEASE AMEND CLAIMS 34, 35, 37 and 38 (MARKED VERSION):

34. (AMENDED) A bond pad structure, comprising:

a semiconductor substrate;

a plurality of conductive [bond pads] regions formed over said semiconductor substrate;

a passivating layer formed over said [bond pads] conductive regions, having multiple openings to each [said bond pads] conductive region;

a barrier layer formed over said passivating layer and in said openings;

a conducting bond pad formed over each said [bond pad] conductive region and over said barrier layer, whereby an upper surface of said conductive bond pad provides improved adhesion for subsequently formed *bonds*.

35. (AMENDED) The bond pad structure of Claim 34, wherein said [conductive] conducting bond pads are formed of copper.

37. (AMENDED) The bond pad structure of Claim 34, wherein said conducting bond pad forms an interlocking grid array in [the] a bond pad via contact region, which is approximately 100 by 100 microns square and the size of the [island] structures are from about 10 to 25 microns in width, approximately 4 microns in height, and from about 4 to 10 in number, per said conducting bond pad, increasing surface area for improved adhesion.

38. (AMENDED) The bond pad structure of Claim 34, wherein said [conductive] conducting bond pads are formed of aluminum.

Amended, New FIGURE

App# 09/442,497 TSMC99-149B

FIG. 5